SVPWM CONTROL OF THREE-PHASE MULTILEVEL DECENTRALIZED POWER CONVERTERS

Phu Cong Nguyen[1,*], Khac Sinh Le[1], Quoc Dung Phan[2]

[1]*Ho Chi Minh City University of Industry and Trade*

[2]*Ho Chi Minh City University of Technology*

[*]Email: *congnp@huit.edu.vn*

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ABSTRACT

This paper presents a method for implementing decentralized space vector pulse width modulation (SVPWM) (DSVPWM) for a three-phase multilevel power converter (TPMPC). The three-phase power converter discussed in this study has a dynamic refactor consisting of multiple cascade modules connected in series in each phase. Each module consists of a cascade dynamic circuit and a local controller. Local controllers will establish a limited number of communications with neighboring controllers, the communication signal used are row and column position cells, reference voltage amplitude, and reference voltage frequency. The DSVPWM method can be considered as a multi-level modulation technique, which can be automatically adjusted based on the number of modules operating in the converter. The execution program of each local module shows a lower number of calculations compared to the power converter using a central controller. The proposed power converter can automatically adjust the dynamic refactoring when a fault occurs to meet the flexibility in control and improve the continuity of power supply in operation. The proposed model and modulation algorithm are analyzed, tested on Matlab/Simulink software.

Keywords: Decentralized control, decentralized SVPWM, multilevel power converter, cascade full bridge converter.

1. INTRODUCTION

The emergence and development of power converters is closely linked to the development of microprocessors. Typically, power converters use a microprocessor as a central controller [1]. As power converters develop, the central processor must increasingly have high processing speed, large connectivity and control capabilities [2]. This is sometimes an obstacle to the design of multi-level power converters and in some cases can lead to quite high processor costs. The core feature when using a central controller is to concentrate all calculations in a single entity. During operation, if an error occurs (loss of connection signal, power error, phase loss, etc.), the system must stop immediately and it takes a relatively long time to re-establish the connection and correct the program. Therefore, flexibility in operation and continuity in power supply may not be achieved. Although it is known that advances in technology and manufacturing techniques allow the production of microprocessors with increasingly high computing speed and connectivity. However, the expansion of control connectivity and processing speed still has certain limitations in the design and manufacture of microprocessors.

The trend of designing power converters in modular form is increasingly interested [3-5]. The modular structure allows power converters to operate flexibly, flexibly in control, easy to maintain and repair when necessary. In the power converter, modules in the form of half bridge [4], full bridge cascade [6], flying capacitor can be connected in series [7,8]. The number of modules connected in series in each phase allows to adjust the voltage amplitude, the number of voltage levels, the switching voltage level... thereby achieving the criteria of voltage quality and power on the load. The pinnacle of the modular structure is used in the decentralized control structure of multilevel power converters. Each module will include a local controller to calculate the necessary switching pulses to directly control the power keys of that module. It can be said that the tasks of the central controller (for centrally controlled

power converters) will be divided for each module in the distributed power converters. Microprocessors with large size, speed and computational capacity are replaced by local processors with low computational requirements and control connectivity [9].

Multilevel modulation techniques have been developed around two main methods: carrier pulse width modulation (CPWM) [10–14] and SVPWM [1,15,16]. The CPWM includes phase shift (PS), phase disposition (PD), phase opposition disposition (POD),... which are processed on an analog technical platform. The switching pulse of each module is calculated and processed in each individual phase of the power converter. Meanwhile, the space vector pulse width dynamic modulation method is processed on a digital platform. The switching pulse of each power switch is calculated in a single central whole, which is convenient for establishing improvements related to the output power quality. Therefore, the SVPWM method shows that it is very suitable for deployment on current microprocessors. The multilevel modulation method using SVPWM technique has been deployed for single phase, three-phase, and multiphase power converter structures; In which, three-phase is the most typical case, with the most applications in industry and civil.

Studies on decentralized control power converters using CPWM have given some very promising results, including: using the PS method for multi-module parallel structures to perform DC/DC modulation [17,18]; using the PS method for multi-module capacitor coupling to perform DC/DC and DC/AC modulation [17,19]; using the PS method for multi-module half bridge and full bridge cascade structures to perform DC/AC modulation [20]. Each module has synthesized for itself carrier waves with appropriate frequencies and amplitudes based on receiving information about carrier amplitude [20], carrier phase angle [18], position... of neighboring modules [20]. Meanwhile, studies on decentralized control power converters using SVPWM have only had some initial results but are very promising and have many prospects in the future.

Based on the structure and the quality index to be achieved, there are many ways to implement SVPWM technique for multilevel power converters. The first method that can be considered is to divide the vector space to be modulated into each modulation region and apply specific algorithms to each modulation region to achieve the desired power quality [21]. This method has the advantage of being able to accurately impact each smallest specific region in the multilevel space vector. However, this leads to a complex calculation process and is often applied to structures with predetermined levels, making it difficult to develop and expand when the number of voltage levels increases. The second method is introduced as a general modulation method for structures with any number of voltage levels [9,22]. This study is conducted by converting the vector space from multilevel to two level vector space, calculating the necessary switching parameters and then converting to multilevel space to determine the required switching vector and switching time. In addition, as the number of modules increases, the number of modulation voltage levels increases, resulting in a very large number of microprocessor calculations. This is a common problem when power converters are designed with a central controller.

This study introduces the connection and control diagram between local controllers; and method of switching pulse modulation for a decentralized TPMPC based on SVPWM technique. The proposed structure and method of DSVPWM show that the computational volume of each local controller is greatly reduced when compared to classical power converters with a central controller. The research proposal allows for quick and convenient dynamic adjustment of the power converter structure to ensure flexibility in control and optimization when necessary. The switching pulses provided to the full bridge cascade power switches are calculated by the local controllers when they aggregate: voltage amplitude and frequency from other controllers; controller position in phase and phase position; total number of controllers that are active. A decentralized three-phase, 13-level cascade converter model is built in Matlab/Simulink software to verify the proposals.

2. THE SVPWM METHOD FOR LOCAL CONTROLLERS OF DECENTRALIZED POWER CONVERTERS

2.1 Proposed structure

Figure 1 shows the interconnection structure of the IGBTs of the cells together, each cell has 4 IGBTs connected in a cascade structure, each cell has used a DC voltage source with a constant amplitude V_{dc}. Meanwhile, a proposed communication proposal for the decentralized control TPMPC

is shown in Figure 2. The number of signals and control functions used by each local controller are shown in Table 1. The *EN* signal enables a cell to work or stop working.

2.2 Proposed SVPWM algorithm

Where i_p is the position information of the cell in the phases, p is the total phases of the inverter (in this study p = 3). To determine the location of the cell in which phase, the study uses a simple sequential numbering method as presented in equations (1), (2). Cells at phase *a* have no information about the previous cell so $i_{p\_in} = 0$.

$$i_{p\_out}^{k} = i_{p\_in}^{k} + 1 \tag{1}$$

$$i_{p}^{k} = i_{p\_out}^{k} \tag{2}$$

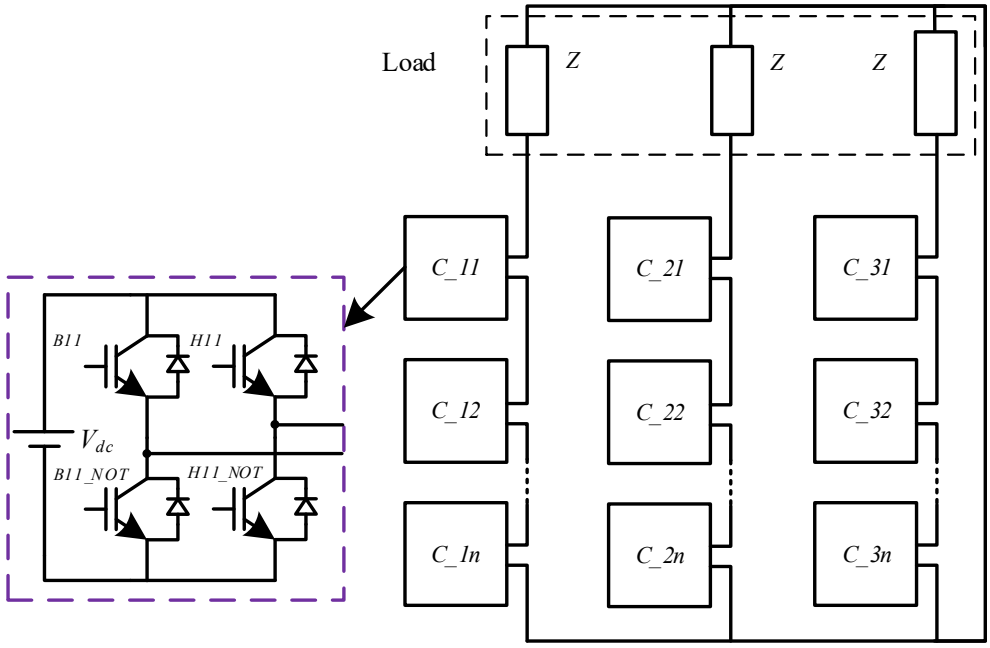


Figure 1. Connection diagram of insulated gate bipolar transistor (IGBT) modules

Table 1. The signal pins of one cell

Symbol	Description
EN	Enable or disable cell operation
V_{rf_in}	Get signal reference voltage from the previous cell
F_{rf_in}	Get reference frequency from the previous cell
i_{n+1}	Get position information from the previous cell in a phase
i_{n-1}	Transmitted position information to the next cell in a phase
i_{p_in}	Get position information from the previous cell in a column
i_{p_out}	Transmitted position information to the next cell in a column
N_{cp_in}	Get total cells information from the previous cell in a phase
N_{cp_out}	Transmitted total cells information to the next cell in a phase
clk_{in}, clk_{out}	Synchronous pulse transmission and reception
V_{rf_out}	Transmitted reference voltage to next cell in a phase
F_{rf_out}	Transmitted reference frequency to the next cell in a phase
$S1, \overline{S1}, S2, \overline{S2}$	The PWM control

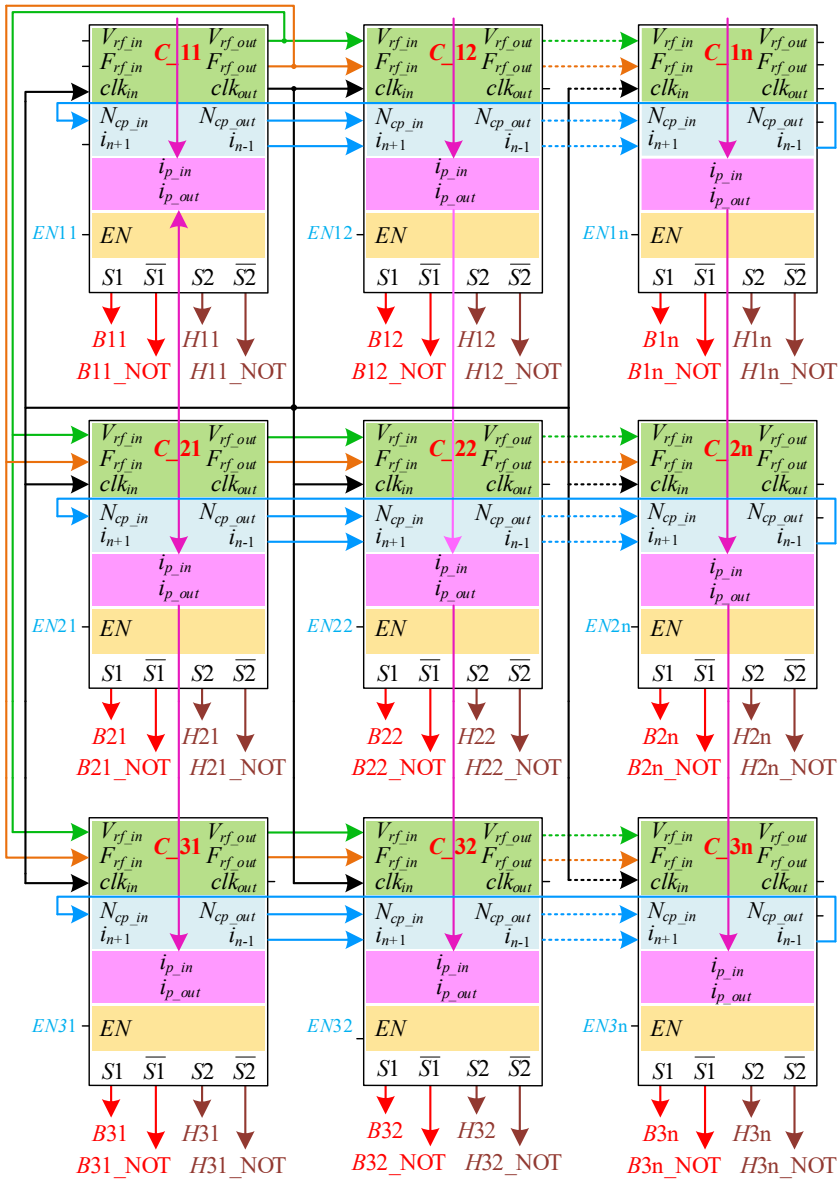


Figure 2. Communication between local controllers with DSVPWM method

A similar procedure is established to calculate the position of cells i_n^k in each phase as shown in equations (3)-(5). The first cell in each phase has no information so $i_{n+1}^k = 0$. The position information of the last cell in each phase is the total active local controllers N_{cp}^k, this signal is transmitted from the first cell to the last cell in each phase.

$$i_{n-1}^k = i_{n+1}^k + 1 \tag{3}$$

$$i_n^k = i_{n-1}^k \tag{4}$$

$$N_{cp}^k = N_{cp\_out}^k = N_{cp\_in}^k \tag{5}$$

The positive-sequence reference voltages for the three-phase multilevel inverter can be expressed by (6), where V_{rf_in} denotes the amplitude of the reference signal:

$$v_{ref}^{k} = \begin{cases} V_{rf\_in} sin(\omega t) \\ V_{rf\_in} sin(\omega t + \frac{2\pi}{3}) \\ V_{rf\_in} sin(\omega t + \frac{4\pi}{3}) \end{cases} \tag{6}$$

Under the multilevel SVPWM scheme, as shown in equation (7), the modulation voltage at the output can be interpreted as an integer multiple of the voltage amplitude provided by a single cell.

$$v_{r}^{k} = \frac{v_{ref}^{k}}{V_{dc}^{k}} = \begin{bmatrix} v_{r1}^{k} & v_{r2}^{k} & v_{r3}^{k} \end{bmatrix}^{T} \tag{7}$$

In equation (8), the floor(x) operator is applied to extract the integer portion of the reference voltage, whereas equation (9) determines its fractional component. The resulting fractional values v_f are then sorted in descending order, as defined in (10).

$$v_{i}^{k} = floor(v_{r}^{k}) \tag{8}$$

$$v_{f}^{k} = v_{r}^{k} - v_{i}^{k} \tag{9}$$

$$v_{fs}^{k} = sort(v_{f}^{k}) = \begin{bmatrix} v_{fs1}^{k} & v_{fs2}^{k} & v_{fs3}^{k} \end{bmatrix}^{T} \tag{10}$$

The matrix A of dimension 1x4 is derived, with its entries determined by expression (11), (12). The matrix D is then introduced as specified in (13).

$$A^{k} = \begin{bmatrix} 0 & A_{2}^{k} & A_{3}^{k} & A_{4}^{k} \end{bmatrix} \tag{11}$$

$$A_{g}^{k} = \begin{cases} 1 \ if \left[v_f \left(i_{p}^{k}, 1 \right) \right] = v_{fs} \left(g, 1 \right) \\ 0 \ if \left[v_f \left(i_{p}^{k}, 1 \right) \right] \neq v_{fs} \left(g, 1 \right) \end{cases} \tag{12}$$

$$with \, g = 2:4$$

$$D^{k} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{13}$$

The switching vector for the 2-level modulation stage is subsequently determined as expressed in (14).

$$v_{d}^{k} = A^{k} D^{k} = \begin{bmatrix} v_{d1}^{k} & v_{d2}^{k} & v_{d3}^{k} & v_{d4}^{k} \end{bmatrix} \tag{14}$$

In the last step, the switching vector v_s is specified by equation (15). The associated switching intervals t_s are subsequently derived from the set of relations given in (16)-(20).

$$v_{s}^{k} = v_{d}^{k} + v_{i}^{k} (i_{p}^{k}, 1) = \begin{bmatrix} v_{s1}^{k} & v_{s2}^{k} & v_{s3}^{k} & v_{s4}^{k} \end{bmatrix} \tag{15}$$

$$t_{s}^{k} = \begin{bmatrix} t_{s1}^{k} & t_{s2}^{k} & t_{s3}^{k} & t_{s4}^{k} \end{bmatrix} \tag{16}$$

$$\sum_{u=1}^{u=p+1} t_{su}^{k} = 1 \tag{17}$$

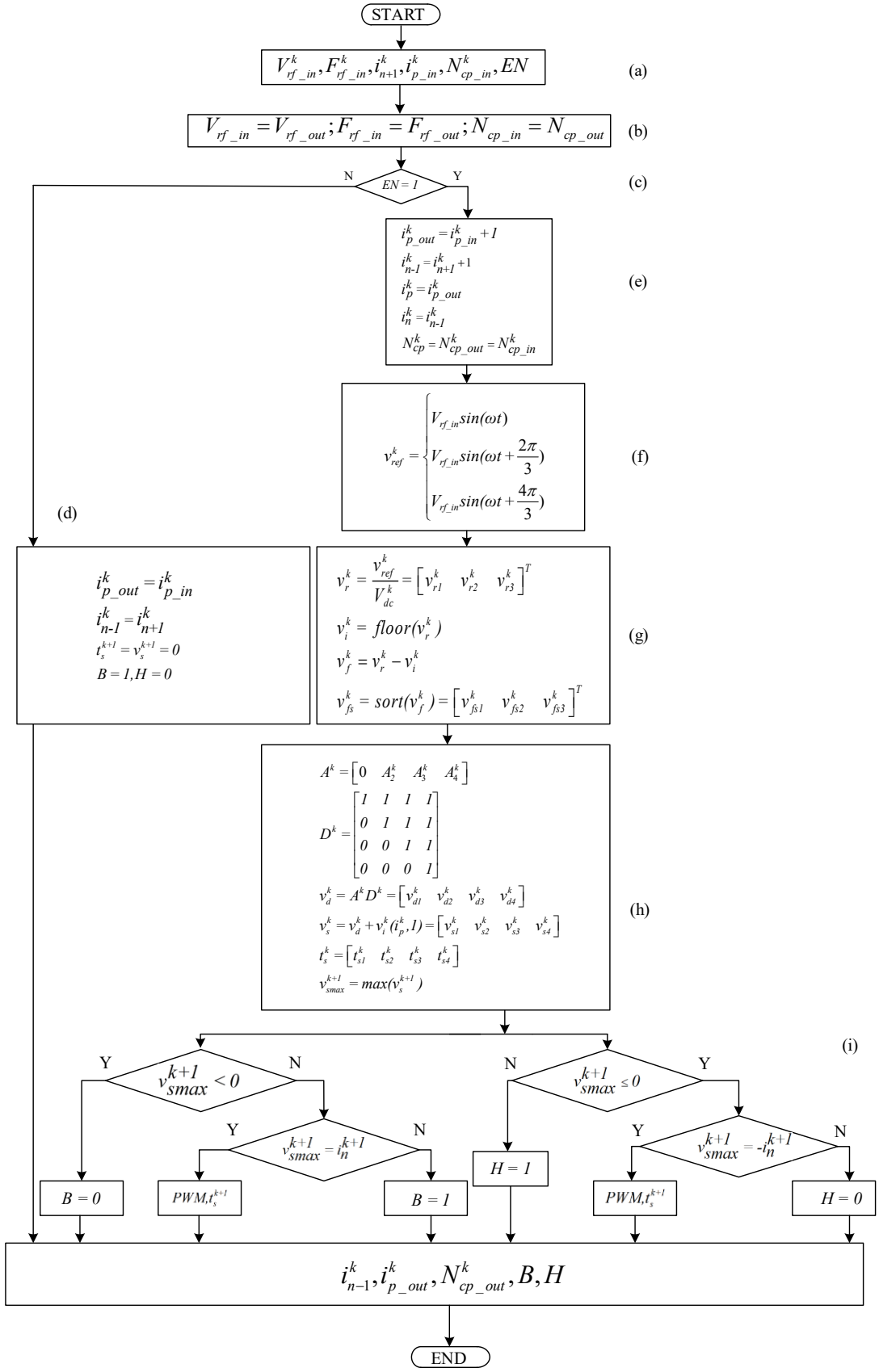


Figure 4. Program execution flowchart of each cell with DSVPWM method

$$t_{s1}^{k} = 1 - v_{fs}^{k}(1,1) \tag{18}$$

$$t_{p+1}^{k} = v_{fs}^{k}(p+1,1) \tag{19}$$

$$t_{j}^{k} = v_{fs}^{k}(j-1,1) - v_{fs}^{k}(j,1) \quad with\ j = 2 \div 3 \tag{20}$$

The largest element in the v_s vector is determined using the function max(x) as (21)

$$v_{smax}^{k} = max\left(v_{s}^{k}\right) \tag{21}$$

$$B = \begin{cases} 0 & if\ v_{smax}^{k} < 0 \\ 1 & if\left(v_{smax}^{k} > 0\right) and\left(v_{smax}^{k} \neq i_{n}^{k}\right) \\ PWM(t_{s}^{k}) & if\left(v_{smax}^{k} > 0\right) and\left(v_{smax}^{k} = i_{n}^{k}\right) \end{cases} \tag{22}$$

$$H = \begin{cases} 1 & if\ v_{smax}^{k} > 0 \\ 0 & if\left(v_{smax}^{k} \leq 0\right) and\left(v_{smax}^{k} \neq -i_{n}^{k}\right) \\ PWM(t_{S}) & if\left(v_{smax}^{k} \leq 0\right) and\left(v_{smax}^{k} = -i_{n}^{k}\right) \end{cases} \tag{23}$$

As depicted in Figure 1, the IGBTs within each module operate according to the control signals defined in equations (22) and (23). A value of B = 1 commands the device to conduct, whereas B = 0 forces it into the non-conducting state. For all other operating modes, the IGBT switching behavior is governed directly by the PWM waveform. The switching sequence of a PWM signal is illustrated in Figure 3, where the corresponding conduction t_{on} and turn-off durations t_{off} are determined using equations (24) and (25).

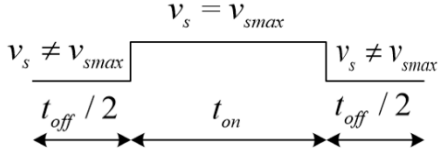


Figure 3. Trigger signal

$$t_{on} = \sum_{u=1}^{u=p+1} t_{su} \quad if(v_{su}^{k} = v_{smax}^{k}) \tag{24}$$

$$t_{off} = 1 - t_{on} \tag{25}$$

In the proposed structure and modulation method, the output voltage is the voltage contribution of the cells that are still operating in the TPMPC, the output phase voltage has the largest amplitude satisfying equation (26). Where *m* be the modulation index, *m* is determined according to equation (27). The control program of each cell is performed according to the algorithm flowchart of Figure 4.

$$v_{out\_\max} = N_{cp} * V_{dc} \tag{26}$$

$$m = \frac{v_m}{V_{dc}} \tag{27}$$

Table 2. The number calculations in a PWM cycle of SVPWM and DSVPWM technique

Calculation process	SVPWM technique	DSVPWM technique
vref	vref is an 3-by-1 matrix	vref is an 3-by-1 matrix.
	$N_{c1} = 3$	$N_{d1} = 3$
vr	vr is an p-by-1 matrix	vr is an 3-by-1 matrix
	$N_{c2} = 3$	$N_{d2} = 3$
vfs	vfs is an 4-by-1 matrix	vfs is an 3-by-1 matrix
	$N_{c3} = 4$	$N_{d3} = 3$
vd	P is an 4-by-4 matrix	A is an 1-by-4 matrix
	$N_{c4} = 4^2$	$N_{d4} = 4$
	Permutation matrix P $N_{c5} = 4^2$	$N_{d5} = 0$
	vd is the product of two matrices 4-by-4	vd is the matrix product of 1-by-4 and 4-by-4
	$N_{c6} = \frac{7}{8}4^3$ $N_{c7} = \frac{7}{8}4^2 2 + \frac{9}{2}4^2$	$N_{d6} = \frac{7}{8}4^2$ $N_{d7} = \frac{7}{8}4*3 + \frac{5}{4}4^2 + \frac{13}{4}4$
	vd is an 3-by-4 matrix	vd is a 1-by-4 matrix
vs	vs is the sum of two matrices 3-by-4	vs is the sum of two matrices 1-by-4
	$N_{c8} = 3*4$	$N_{d8} = 4$
	vs is an 3-by-4 matrix	vs is a 1-by-4 matrix
ts	ts is an 3-by-4 matrix	ts is a 1-by-4 matrix
	$N_{c9} = 3*4$	$N_{d9} = 4$

2.3 Evaluation of the computational requirements per PWM cycle for SVPWM and DSVPWM schemes

Expressions (28) and (29) [23] specify the number of arithmetic operations involved in multiplying and adding the matrices A(x,y) and B(y,z). Using these expressions, Table 2 presents the computational requirements for each modulation stage of the conventional SVPWM method [24] and the proposed DSVPWM scheme. The results indicate that one switching cycle of SVPWM requires a total of 222 calculations, whereas the proposed method completes the cycle with only 64 calculations. This corresponds to a reduction in computational effort by a factor of about 3.5.

$$N_{mul} = \frac{7}{8}xyz \tag{28}$$

$$N_{add} = \frac{7}{8}x(y-2)z + \frac{5}{4}xy + \frac{5}{4}yz + \frac{8}{4}xz \tag{29}$$

3. SIMULATION RESULTS AND DISCUSSION

3.1 Configuration and simulation parameters

The three-phase, 13-level power converter is built on Matlab software; each phase has 6 full cells connected in series; Simulation parameters are shown in Table 3. Simulations of TPMPC operation to analyze the main issues:

- The ability to automatically configure the system in the normal operating state, the cells will accurately determine their own position in the phases and the phase position that the cell is locating.

- The system can accurately construct the output voltage so that it matches the prescribed reference voltage.

Table 3. Simulation parameters

Parameter	Symbol	Unit	Value
DC voltage of each cell	Vdc	V	100
Modulation index	m		5.8
Load	L	H	0.01
	R	Ω	10
Switching frequency	fsw	kHz	10
Reference frequency	Frf	Hz	50
Sampling time	Ts	s	10^{-6}

- The system is capable of automatically adapting its dynamic refactoring when cells are added to or removed from the phases. Each cell updates its position within the corresponding phase, along with the information regarding the total number of active cells. As a result, the output voltage is synthesized accurately based on the voltage contribution of each active cell.

3.2 Simulation results

Figure 5 shows the process of cells determining their own positions in phases and columns. After three calculation steps, the cells have determined their phase positions, and after six calculation steps, the cells have determined their own positions in cells.

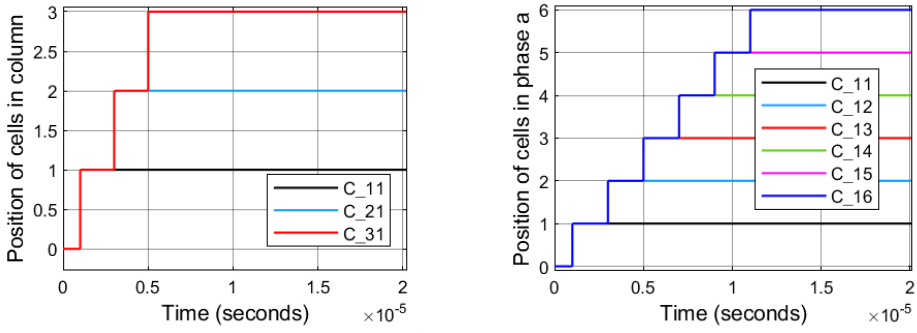
In the structure of a TPMPC, the number of cells in each phase is usually larger than the number of phases, so the time it takes for the system to complete configuration from start-up may be calculated by the number of cells in the phases. Therefore, the configuration time of the N_c system can be calculated as equation (30).

$$N_c = N_{cp} \tag{30}$$

At start-up, the power converter operates with full cells, modulation index m = 5.8, reference frequency is 50Hz. Then, the simulation process is carried out as described in Figure 6. Figure 7 presents the simulation results showing the cell positions in phase and column, phase voltage and load current waveforms. With six cells contributing to each phase, the output phase voltage achieves 13 distinct levels, and its frequency responds exactly to the specified reference frequency.

At 0.04 seconds, three cells C_13, C_23, C_33 stop working, the signals to the stopped cells will be transmitted directly from the input to the output, the 5 active cells in each phase quickly adjust their own positions, re-determine the appropriate switching vectors and switching times. The output phase voltage has 11 levels as the voltage contribution of the 5 cells, the maximum reference voltage amplitude that can be achieved is 500V.

The simulation results show that the voltage switches to a stable new state very quickly, and the transition process has no significant impact on the required voltage quality.



a) b)

Figure 5. Position of cells; a) Position of cells *C_11, C_21, C_31*; b) Position of cells *C_11, C_12, C_13, C_14, C15, C_16*.

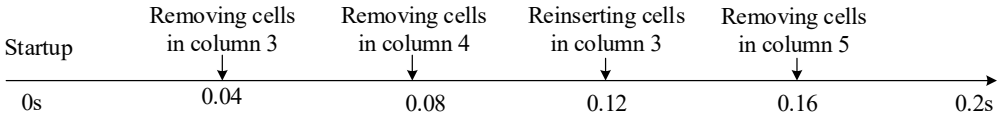


Figure 6. Simulation process

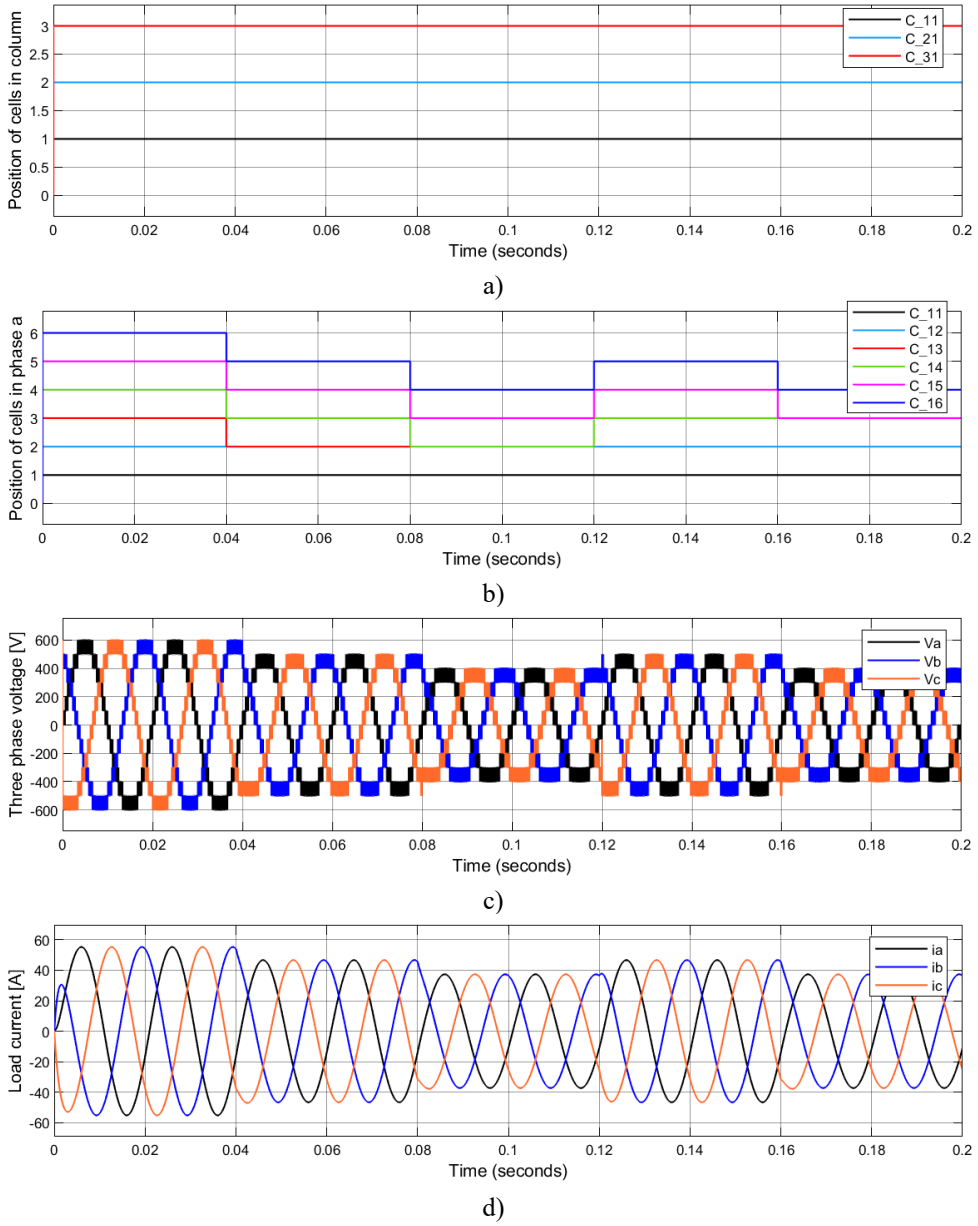


Figure 7. Simulation results in case of dynamic restructuring; a) Position of cells *C_11, C_21, C_31*; b) Position of cells *C_11, C_12, C_13, C_14, C15, C_16*; c) Three-phase voltage; d) Load current

At 0.08 seconds, four cells *C_14, C_24, C_34* continue to be removed, the remaining cells in the phases quickly adjust to the new state, the position of cell *C_11* is 1, the position of cell C_12 is 2, the position of cell C_15 is 3, the position of cell C_16 is 4, as shown in Figure 7a. The remaining phase voltage is a maximum of 400V, there are 9 levels, the difference between the levels is still exactly 100V, the voltage frequency responds exactly to the reference frequency of 50Hz. This simulation result also

shows the same in the period from 0.16 seconds to 0.2 seconds when the TPMPC has 4 active cells in each phase.

At 0.12 seconds, the cells *C_13, C_23, C_33* are reinserted to continue working, each phase has 5 active cells, the output voltage has 11 levels, the position of the cells is quickly adjusted and rearranged from 1 to 5, the voltage between two levels is still stable with a value of 100V.

The tests have shown that during operation, the DSVPWM method and the proposed structure can ensure that the system performs dynamic refactoring, the TPMPC does not require to stop operating. This is one of the factors affecting the reliability and operation of the energy conversion system.

4. CONCLUSIONS

The decentralized three-phase multilevel power converter using SVPWM method has been successfully used to find the switching pulse for each local cell. The calculation program of each cell shows a significant reduction in the amount of calculations when compared to the use of a central controller, which opens up the prospect of using low-speed and low-computation microprocessors in the design of power converters. The proposed decentralized power converter also shows the ability to automatically adjust the dynamic refactoring in case of adding or removing a cell, which contributes to increased operational flexibility and reliability in the ability to provide continuous, uninterrupted power. The content presented in this paper is limited to the analysis and evaluation on the simulation model. This research direction will continue to be considered and implemented on the experimental model, the detailed analysis and evaluation when implemented on the experimental model will be conducted and published in the coming time.

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TÓM TẮT

ĐIỀU KHIỂN CÁC BỘ BIẾN ĐỔI CÔNG SUẤT PHÂN TÁN BA PHA ĐA BẬC DÙNG SVPWM

Nguyễn Phú Công[1,*], Lê Khắc Sinh[1], Phan Quốc Dũng[2]

[1]Trường Đại học Công Thương Thành phố Hồ Chí Minh

[2]Trường Đại học Bách Khoa Thành phố Hồ Chí Minh

*Email: *congnp@huit.edu.vn*

Bài báo này trình bày cách thức triển khai phương pháp điều chế độ rộng xung vec-tơ không gian phân tán (SVPWM) (DSVPWM) cho các bộ biến đổi công suất ba pha, đa bậc (TPMPC). Bộ biến đổi công suất ba pha được đề cập trong nghiên cứu này có cấu hình mạch bao gồm đa mô-đun cascade ghép nối tiếp trong mỗi pha. Mỗi mô-đun bao gồm một mạch động lực cascade và một bộ điều khiển cục bộ. Các bộ điều khiển cục bộ sẽ trao đổi thông tin hạn chế với các mô-đun lân cận, thông tin giao tiếp có thể là vị trí mô-đun theo hàng và theo cột, biên độ điện áp tham chiếu, tần số của điện áp tham chiếu. Phương pháp DSVPWM có thể được xem xét như là một kỹ thuật điều chế đa bậc, phương pháp có thể tự động điều chỉnh dựa trên số lượng mô-đun đang hoạt động trong hệ thống. Chương trình thực thi của mỗi mô-đun cục bộ cho thấy số lượng phép tính thấp hơn so với bộ biến đổi công suất sử dụng một bộ điều khiển trung tâm. Bộ biến đổi công suất đề xuất có thể tự động điều chỉnh cấu trúc động khi có lỗi xảy ra nhằm đáp ứng tính linh hoạt trong điều khiển và nâng cao tính liên tục cung cấp điện trong vận hành. Cấu trúc và giải thuật điều chế đề xuất được tiến hành đánh giá trên phần mềm mô phỏng Matlab/Simulink.

Từ khóa: Điều khiển phân tán, điều chế độ rộng xung vec-tơ không gian phân tán, bộ biến đổi công suất đa bậc, bộ biến đổi công suất nối tầng.